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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/382,677	08/25/1999	MASAAKI HIROKI	0756-2016	5550

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EXAMINER	
TRAN, HENRY N	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/382,677	HIROKI, MASAAKI	
	Examiner	Art Unit	
	Henry N. Tran	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-7,8/2,9/2,10/2,11/2,3,8/3,9/3,10/3,11/3,13,16-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,8/3,9/3,10/3,11/3,30-34* is/are allowed.

6)☒ Claim(s) *2,5-7,8/2,9/2,10/2,11/2,13,17-29* is/are rejected.

7)☒ Claim(s) *4 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Response received May 2, 2005 has been fully considered; and this Office action is in response thereto.

Claims 2-11, 13 and 16-34 remain pending in this application.

Response to Arguments

2. Applicant's arguments, see pages 1-9 of the Response, filed 5/2/05, with respect to the rejections of: claims 5-7 and 17-19 under 35 U.S.C. 112, first paragraph; the rejections of claims 13 and 17 under 35 U.S.C. 102(e); and the rejections of claims 2-11, 16, 18-34 have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. However, upon further consideration, new grounds of rejection are made in view of Eglit (U.S. Patent No. 6,320,574), and Shigeta (U.S. Patent No. 6,657,640).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 5-7, 8/2, 9/2, 10/2, 11/2, 13 and 17-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eglit (U.S. Patent No. 6,320,574) in view of Shigeta (U.S. Patent No. 6,657,640).

6. Regarding claim 2, Eglit, Fig. 8, teaches a method of driving a display device 100, comprising the steps of: frequency modulating a reference clock signal and obtaining a

modulated clock signal; performing sampling and A/D conversion on an analog image signal on the basis of the modulated clock signal for obtaining a digital image signal, and performing digital signal processing on the digital image signal; and supplying the image signal to a corresponding pixel and obtaining an image (Eglit teaches that a clock generator 850 is used for receiving a reference clock signal 802, which is a HSYNC signal, which is then frequency modulated for providing a modulated signal (Eglit calls "a sampling clock signal") on line 851 to ADC 810 for performing sampling on an analog image signal provided to the ADC 810 on line 801 and obtaining a digital image signal on line 812 for processing for obtaining an image on a display screen 100), see also, Figs. 1A and 1B, col. 6, line 45 to col. 7, line 17.

However, Eglit does not teach that the step of performing D/A conversion on the digital image signal on the basis of the reference clock signal and obtaining an improved analog image signal for supplying to a corresponding pixel and obtaining an image.

Shigeta, Fig. 2, teaches that a D/A converter 4 is used for performing the method step of performing D/A conversion on a digital image signal provided by an image processing unit 3 on the basis of the display resolution and obtaining an improved analog image signal for supplying to a corresponding pixel and obtaining an image, see also, Figs. 3 and 4, col. 3, line41 to col. 4, line 2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the step of performing D/A conversion on a digital image signal as taught by Shigeta in the Eglit method steps, wherein, the Shigeta display resolution is corresponding to the Eglit reference clock signal because this would provide an improved display driving method capable of driving display units having different resolutions at low cost, see Shigeta, col. 4, lines 13-15.

7. Regarding claims 5-7 and 8/2, 9/2, 10/2 and 11/2, Eglit further teaches that: (i) the modulated clock signal is obtained by randomly shifting a frequency of the reference clock signal (clock signals may have different frequencies ...synchronized with time reference signal by divided by K), see col. 5, lines 27-33; and col. 7, lines 2-6; (ii) the modulated clock signal is obtained by shifting a frequency of the reference clock signal in the form of a sine wave or a triangular wave, see col. 10, lines 59-60; (iii) the display device is an active matrix or a passive matrix type liquid crystal display device, see col. 7, lines 18-21. Shigeta further teaches that the display device is an electroluminescent device such as a FED (Field Emission Device); see col. 2, lines 51-54.

Claims 5-7, 8/2, 9/2, 10/2, 11/2 are dependent upon the base claim 2; and are therefore rejected on the same reasons set forth in claim 2, and by the reasons discussed above.

8. Regarding claim 13, Eglit, Fig. 8, teaches a modulated clock signal obtained by frequency modulating a reference clock signal as discussed for claim 2 above (see paragraph 6); and a VSYNC signal is provided to the clock generator 850 for producing a modulated VSYNC signal to a panel interface 830 for driving the display screen 100 (Eglit teaches that a clock generator 850 is used for receiving a reference clock signal 802, which is a VSYNC signal, which is then frequency modulated for providing a modulated clock signal provided to the panel interface 830 for processing processed digital signals for obtaining an image on a display screen 100), see also, Figs. 1A, col. 7, lines 1-17. Shigeta teaches that the display device comprising: an active matrix circuit having a plurality of thin-film transistors 19 arranged in a matrix form, and a source signal line-side driving circuit 9 and a gate signal line-side driving circuit 12 for driving said active matrix circuit, wherein a horizontal shift clock signal, ϕHCK 11, is inputted to said

source signal line-side driving circuit, while a vertical shift clock signal, ϕVCK 14, which differs from said horizontal shift clock signal in quantity of frequency shifting, is inputted to said a gate signal line-side driving circuit. Accordingly, as discussed for claim 2 above, the modulated clock signal that is a sampling clock signal is corresponding to the horizontal shift clock signal ϕHCK 11, and the modulated clock signal VSYNC is corresponding to the vertical shift clock signal ϕVCK 14. By this rationale, claim 13 is rejected.

9. Regarding claims 17-21, which comprise similar claim limitations recited for claims 5-7 and 10-11, and are rejected based on the same basis set forth in claims 5-7 and 10-11 discussed above (see paragraph 7).

10. Regarding claims 22-29, which depend upon the base claim 13, rephrased to claim that the display device is used in different electronic apparatus. Eglit further teaches that the display could be used in any graphics system having a display unit; see col. 5, lines 40-45. Shigeta further also teaches that that the display could be used in any image display apparatus; see col. 2, lines 51-56. Claims 22-29 are therefore rejected on the same reasons set forth in claim 13, and by the reasons noted above.

Allowable Subject Matter

11. Claims 3, 8/3, 9/3, 10/3, 11/3 and 30-34 are allowed.

12. Claims 4 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. They are:

- Mizukata et al. (U.S. Patent No. 6,020,872) teach a matrix type display system that uses different modulated clock signals for sampling an analog display signal; and
- Chiang (U.S. Patent No. 6,271,822) teach a matrix type display system having a D/A converter for performing D/A conversion on the digital image signal.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry N. Tran whose telephone number is 571-272-7760. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RICHARD A. HJERPE can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Henry N. Tran

Henry N Tran
Primary Examiner
Art Unit 2674

HT
3/13/06